



FIG. 1 (a)

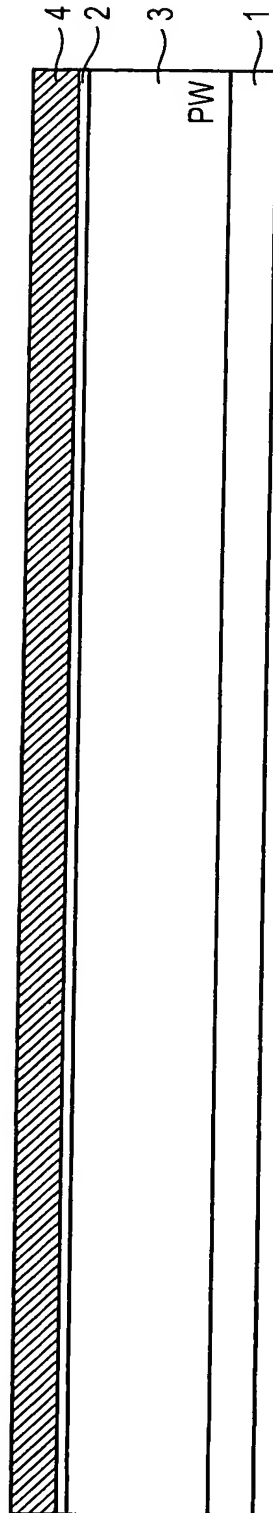
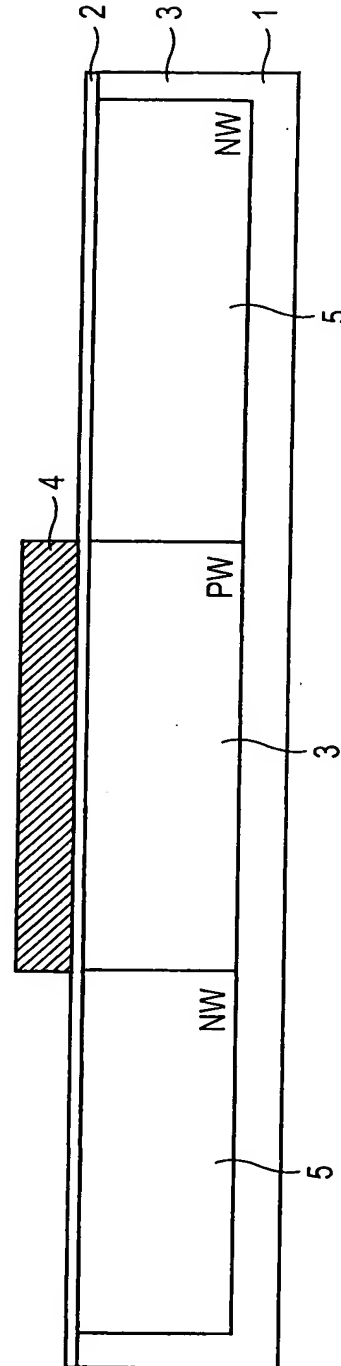


FIG. 1 (b)



2/14

FIG. 2 (a)

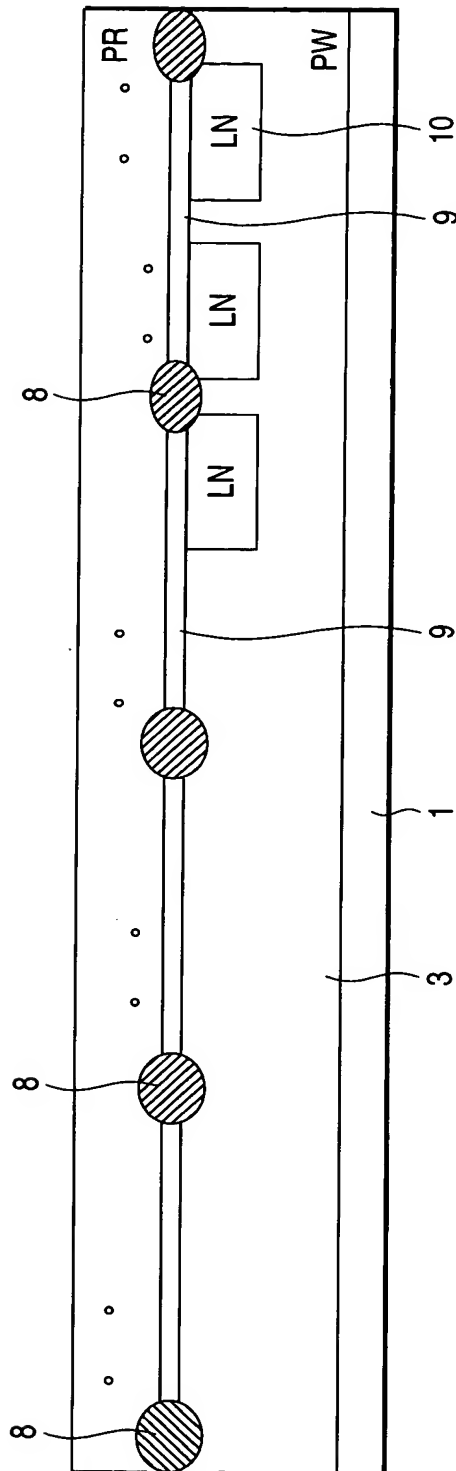
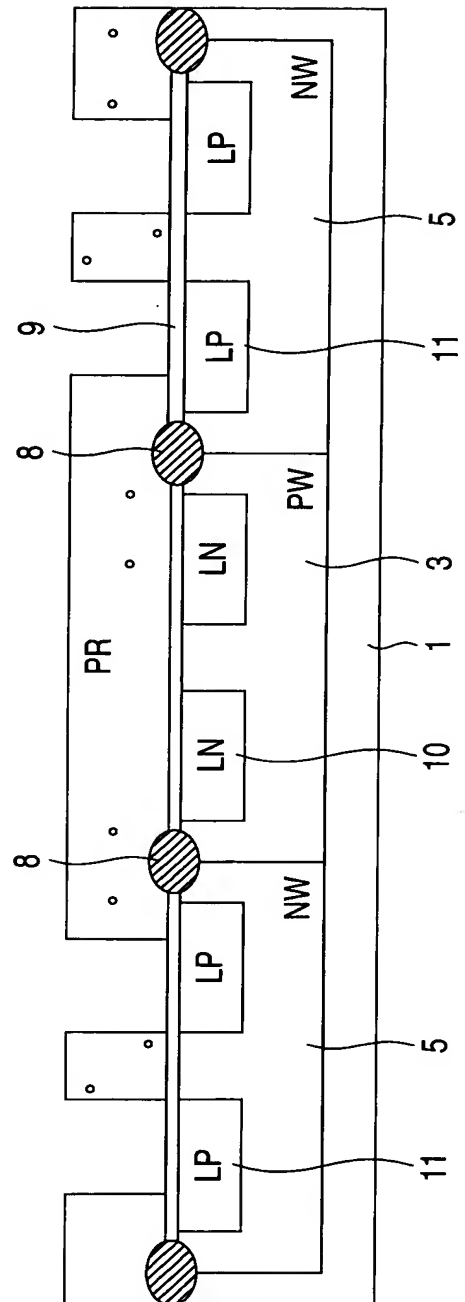


FIG. 2 (b)



3/14

FIG. 3 (a)

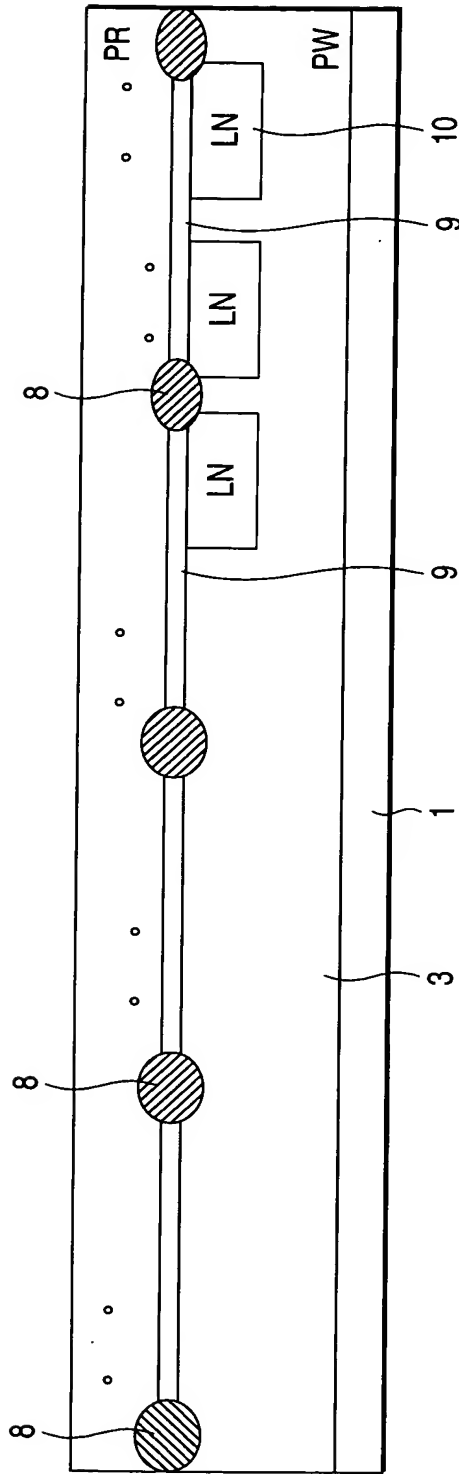
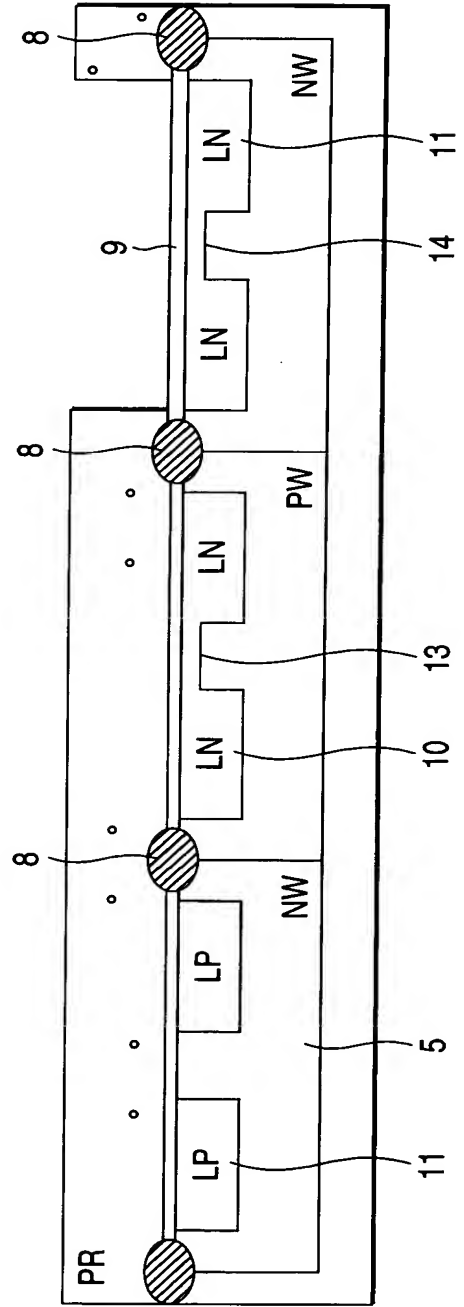


FIG. 3 (b)



4/14

FIG. 4 (a)

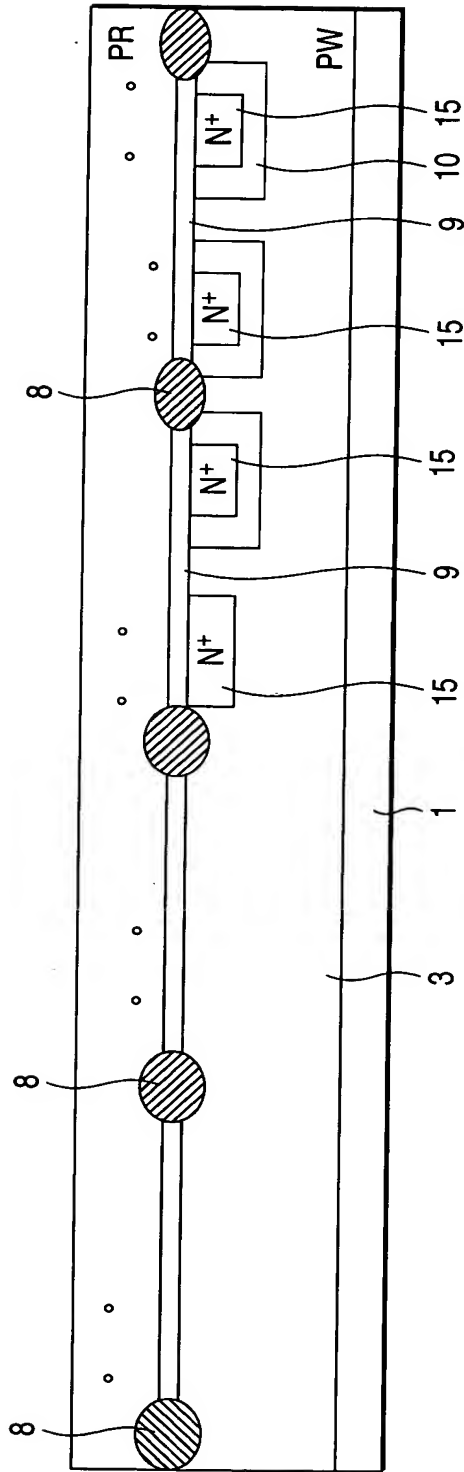
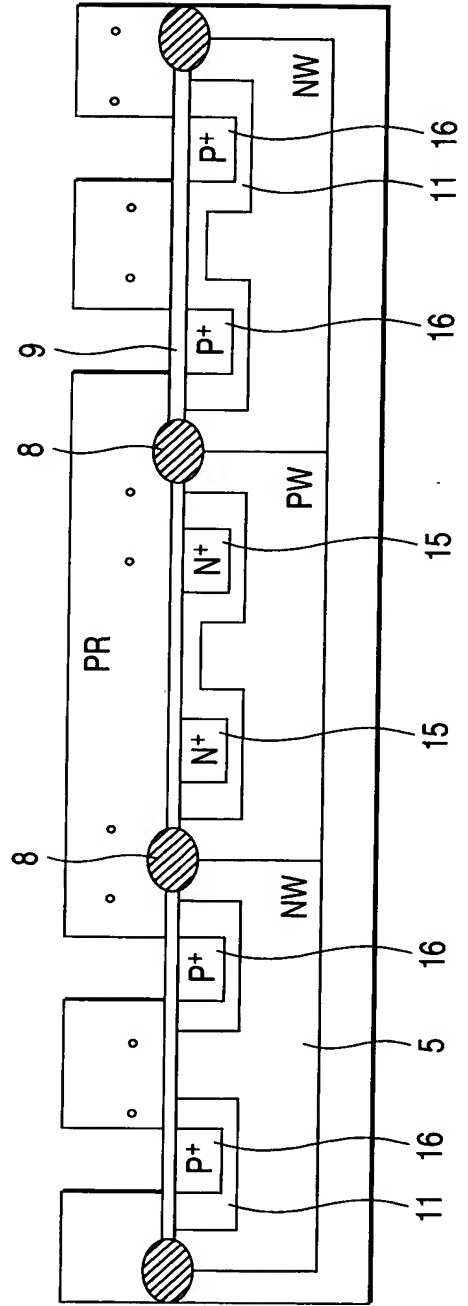


FIG. 4 (b)



5/14

FIG. 5 (a)

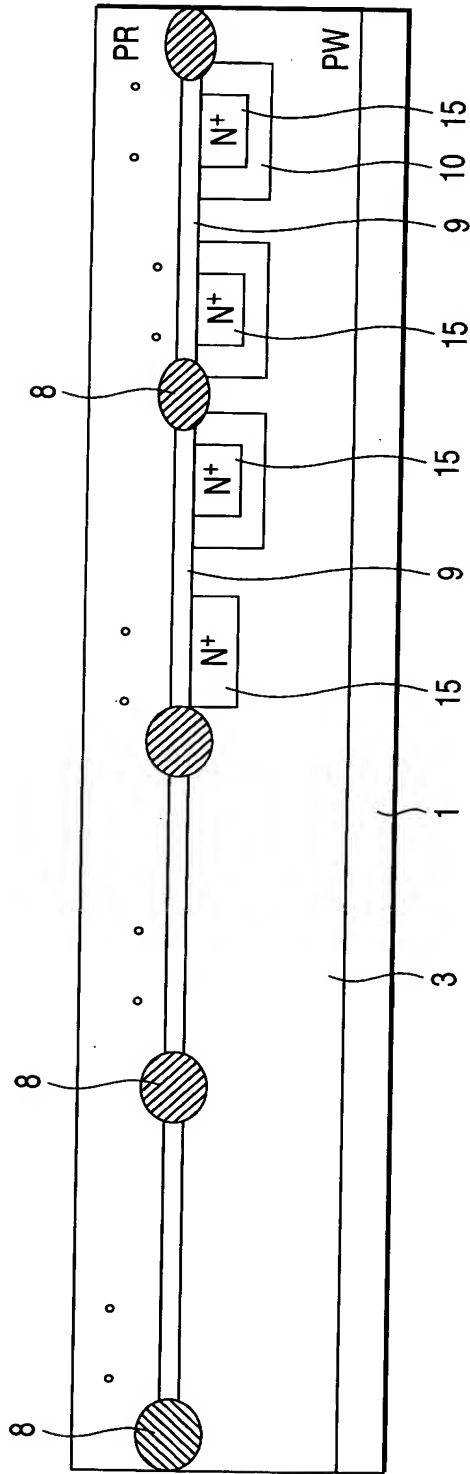
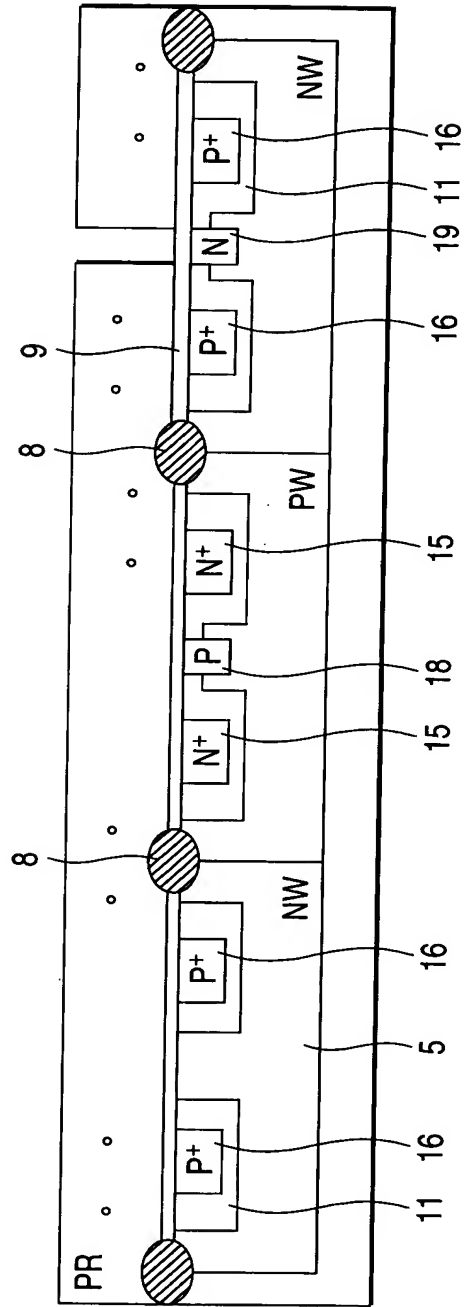


FIG. 5 (b)



This diagram shows a cross-sectional view of a semiconductor device. A central channel is defined by a layer labeled 8. On either side of this channel are regions labeled PR and SNW. The device includes several N+ regions, with labels 15 and 9 indicating specific areas. A PW region is also shown. The device is built on a substrate labeled 21. The channel 8 is connected to a terminal labeled 22. The PR and SNW regions are connected to a terminal labeled 3. The N+ regions are connected to a terminal labeled 1. The PW region is connected to a terminal labeled 15. The device is shown in a perspective view, with the channel 8 and the N+ regions being the primary features.

This diagram shows a cross-sectional view of a semiconductor device. It features a substrate 5 with a channel layer 11. Above the channel layer, there are four gate regions labeled PR, NW, PW, and NW. The device includes various doped regions: P<sup>+</sup> regions 16, N<sup>+</sup> regions 15, P regions 18, and N regions 19. A P<sup>+</sup> region 20 is located at the top. Shaded circles represent contacts or vias. The device is divided into sections by vertical lines, with labels 8 and 9 indicating specific regions.



[illegible]

This cross-sectional view shows a semiconductor device with a substrate 5. Four gate regions, labeled 27E, 27F, 27G, and 27H, are positioned along the top surface. Each gate region is associated with a specific doped region: P+ (11) under gate 27E, N+ (15) under gate 27F, P+ (16) under gate 27G, and N+ (19) under gate 27H. The device also includes NW (Not Work) regions and PW (Passive Work) regions. The regions are separated by insulating layers 8. The labels 11, 15, 16, and 19 are placed at the bottom of the diagram, corresponding to the P+ and N+ regions.



This cross-sectional view shows a semiconductor device with a substrate 1. A thin layer 9 is on top of the substrate. A layer 15 contains several regions: N<sup>+</sup> regions 15, P<sup>-</sup> regions 29, and SNW regions 28. A layer 8 is on top of layer 15. A layer 24 is on top of layer 8. A layer 27 is on top of layer 24. A layer 27A is on top of layer 27. A layer 27B is on top of layer 27A. A layer 27C is on top of layer 27B. A layer 27D is on top of layer 27C. A layer PR is on top of layer 27D. A layer PW is on top of layer PR. A layer 28 is on top of layer PW. A layer 29 is on top of layer 28. A layer 15 is on top of layer 29. A layer 9 is on top of layer 15. A layer 1 is on top of layer 9.

This diagram shows a cross-section of a semiconductor device with three repeating unit regions labeled 27E, 27F, and 27G. Each region contains a P<sup>+</sup> layer (16), an N<sup>+</sup> layer (15), and a P layer (18). The regions are separated by NW (Notch Width) and PW (Pitch Width) dimensions. A PR (Passivation Layer) is shown at the bottom, and a hatched layer is on top.

This diagram shows a cross-sectional view of a semiconductor device. It features a substrate with multiple layers and regions. Key components include:
 

- SPW** (Source/Pad/Well) and **SNW** (Source/Node/Well) regions, which are  $N^+$  doped regions.
- P+** doped regions, likely for contacts or gates.
- 27A** and **27B** are gate structures or spacers.
- 27C** and **27D** are additional gate or spacer structures.
- PR** (Photoresist) is shown on top of the device.
- PW** (Passivation/Protective) is the topmost layer.
- 8** indicates specific nodes or contact points.
- 30** and **31** are labels for various layers or regions.
- 15** and **9** are additional labels for layers or regions.

11/14

FIG. 11 (a)

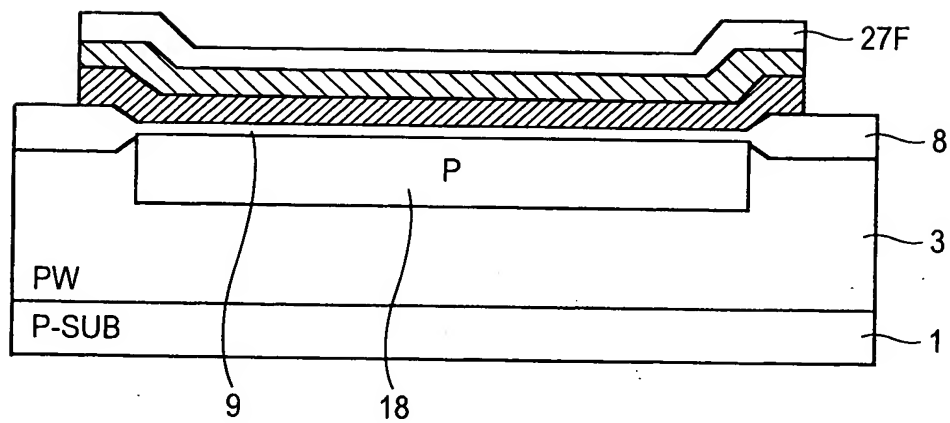
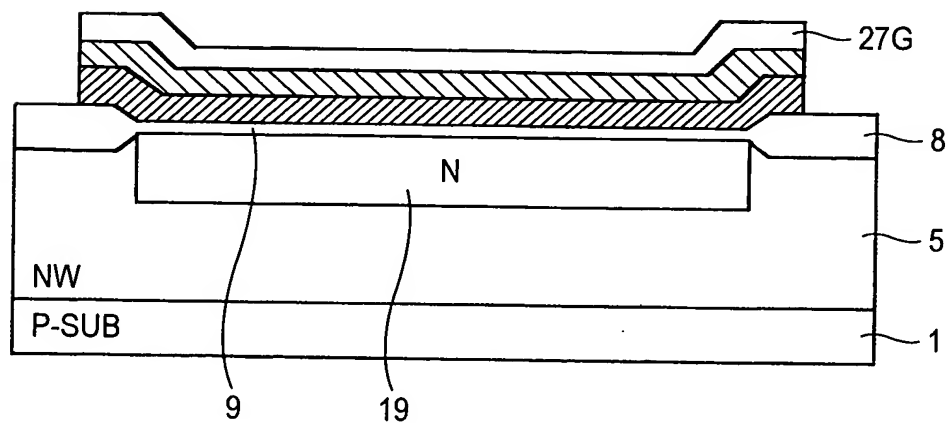


FIG. 11 (b)



12/14

FIG. 12 (a)

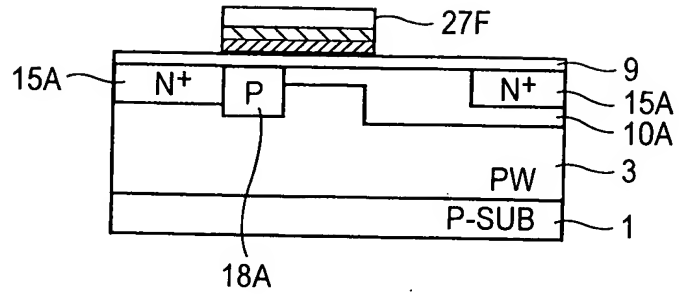
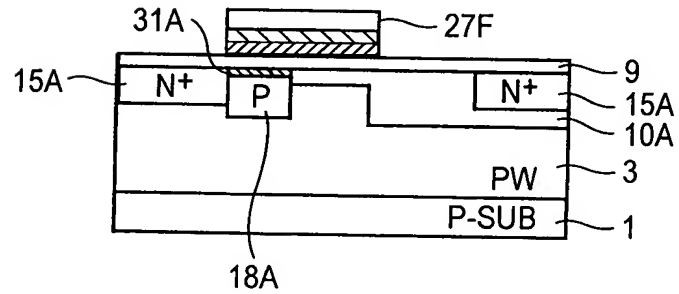


FIG. 12 (b)



13/14

FIG. 13 (a)

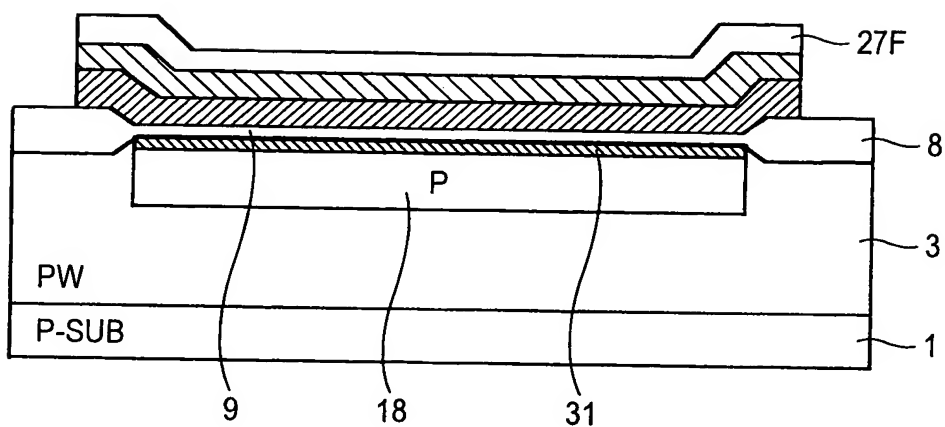
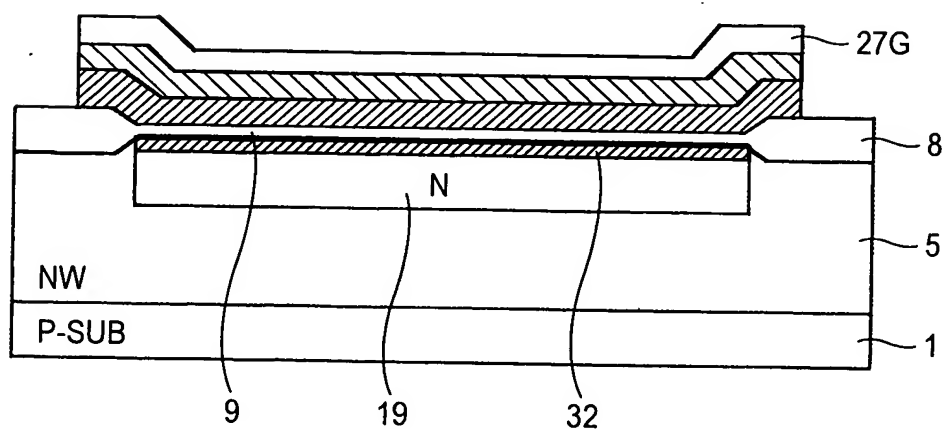


FIG. 13 (b)



14/14

FIG. 14

